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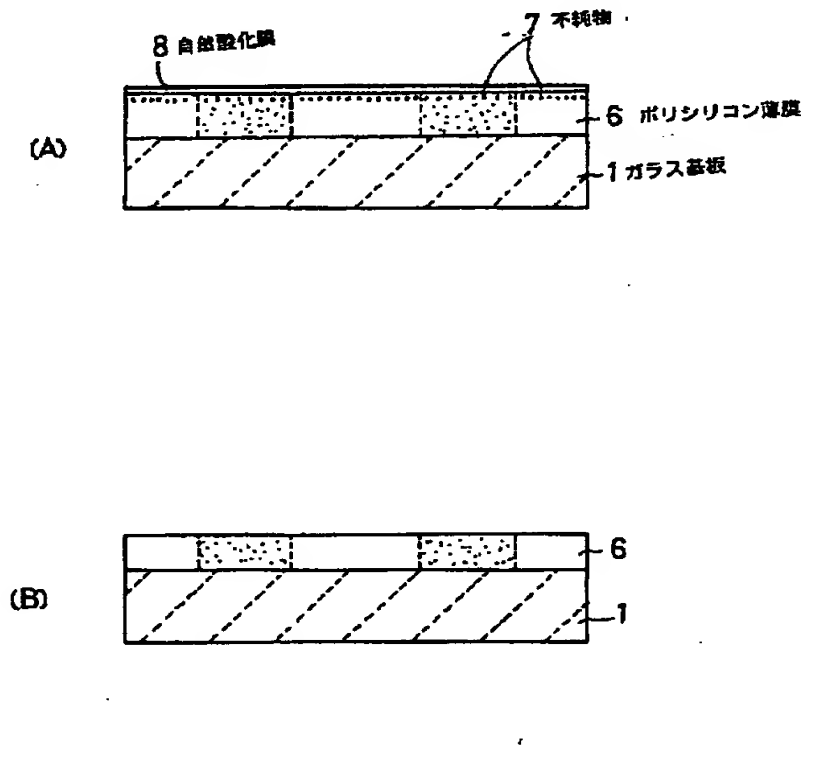
(54)【発明の名称】薄膜トランジスタの製造方法

(57)【要約】
【目的】　ポリシリコン薄膜の膜質を良くする。
【構成】　ガラス基板１の上面にアモルファスシリコン薄膜を目的とする膜厚よりも１００Å程度厚く形成する。次に、エキシマレーザを照射すると、アモルファスシリコン薄膜がポリ化してポリシリコン薄膜６となる。次に、ポリシリコン薄膜６の膜質を安定化するために、窒素雰囲気中において熱処理を行うと、ポリシリコン薄膜６の表面に自然酸化膜８が形成される。次に、１％フッ酸に１分間程度浸し、エッチングを行う。すると、自然酸化膜８が数秒間程度で除去され、この後ポリシリコン薄膜６の表面層が１００Å程度除去される。これにより、レーザアニールにより溶融したアモルファスシリコン薄膜がガラス基板１側から凝固してポリ化し、アモルファスシリコン薄膜中に存在する不純物７がポリシリコン薄膜６の表面層に集中して残留していても、この残留する不純物７が除去されることになる。



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【特許請求の範囲】

【請求項１】　基板上に形成された半導体薄膜をレーザアニールした後、前記半導体薄膜の表面層を該表面層に集中した不純物と共に除去することを特徴とする薄膜トランジスタの製造方法。

【請求項２】　前記半導体薄膜は前記レーザアニール前アモルファスシリコン薄膜であって、前記レーザアニールにより該アモルファスシリコン薄膜をポリ化することを特徴とする請求項１記載の薄膜トランジスタの製造方法。

【請求項３】　前記レーザアニール後に熱処理を施し、この後前記半導体薄膜の表面層を除去することを特徴とする請求項１記載の薄膜トランジスタの製造方法。

【請求項４】　前記熱処理は窒素雰囲気中で行うことを特徴とする請求項３記載の薄膜トランジスタの製造方法。

【請求項５】　前記熱処理は酸素雰囲気中で行うことを特徴とする請求項３記載の薄膜トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は薄膜トランジスタの製造方法に関する。

【０００２】

【従来の技術】薄膜トランジスタの製造分野では、ガラス基板上に形成したアモルファスシリコン薄膜を、レーザアニールすることにより、ポリ化してポリシリコン薄膜とすることがある。この場合、レーザアニールにより溶融したアモルファスシリコン薄膜がガラス基板側から凝固してポリ化する。また、イオン注入後のポリシリコン薄膜をレーザアニールして活性化することもあるが、この場合もレーザアニールにより溶融したポリシリコン薄膜がガラス基板側から凝固する。

【０００３】

【発明が解決しようとする課題】このように、レーザアニールにより溶融したアモルファスシリコン薄膜等からなる半導体薄膜がガラス基板側から凝固するので、半導体薄膜中に存在する不純物がその表面層に集中して残留することになる。この結果、このような構造の半導体薄膜を備えた薄膜トランジスタでは、半導体薄膜の膜質が良くなく、オン電流、オフ電流、しきい値電圧等の電気的特性が劣化するという問題があった。この発明の目的は、半導体薄膜の膜質を良くすることのできる薄膜トランジスタの製造方法を提供することにある。

【０００４】

【課題を解決するための手段】この発明は、基板上に形成された半導体薄膜をレーザアニールした後、前記半導体薄膜の表面層を該表面層に集中した不純物と共に除去するようにしたものである。

【０００５】

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【作用】この発明によれば、半導体薄膜の表面層を該表面層に集中した不純物と共に除去することになるので、半導体薄膜の膜質を良くすることができる。

【０００６】

【実施例】図１～図８はそれぞれこの発明の一実施例における薄膜トランジスタの各製造工程を示したものである。そこで、これらの図を順に参照しながら、薄膜トランジスタの製造方法について説明する。

【０００７】まず、図１に示すように、ガラス基板１の上面にSiH_4とH_2との混合ガスを用いたプラズマＣＶＤにより水素化アモルファスシリコン薄膜２を堆積する。この場合、水素化アモルファスシリコン薄膜２の膜厚が目的とする膜厚よりもある程度厚くなるようにする。例えば、目的とする膜厚が５００Å程度であるならば、プラス１００Åの６００Å程度とする。また、堆積条件としては、ガラス基板１の温度を２００～３５０℃程度望ましくは２５０℃程度とし、１０～２０ＳＣＣＭ程度のSiH_4とその１０倍程度のH_2との混合ガスを用いる。すると、水素化アモルファスシリコン薄膜２の水素含有量は１０～２０ａｔｏｍｉｃ％程度となる。次に、後の工程でエキシマレーザ照射により高エネルギを与えたとき水素が突沸して欠陥が生じるのを回避するために、脱水素処理を行う。この場合、窒素雰囲気中において４５０℃程度の温度で１時間程度の熱処理を行い、水素含有量が３ａｔｏｍｉｃ％以下望ましくは１ａｔｏｍｉｃ％以下となるようにする。

【０００８】次に、図２に示すように、脱水素処理後のアモルファスシリコン薄膜３のソース・ドレイン形成領域３ａ以外の領域に対応する部分の上面にフォトレジスト膜４を形成する。次に、このフォトレジスト膜４をマスクとしてアモルファスシリコン薄膜３のソース・ドレイン形成領域３ａにリンイオンやボロンイオン等のイオンを注入してイオン注入領域５を形成する。この後、フォトレジスト膜４を除去する。

【０００９】次に、図３に示すように、真空中において基板温度２００～４００℃で波長３０８ｎｍのＸｅＣｌエキシマレーザをエネルギ密度２５０～３５０ｍＪ／ｃｍ²程度、パルス幅５０ｎｓｅｃ程度で照射すると、アモルファスシリコン薄膜３がポリ化してポリシリコン薄膜６になると同時にイオン注入領域５が活性化される。この場合、レーザアニールにより溶融したアモルファスシリコン薄膜３がガラス基板１側から凝固することにより、アモルファスシリコン薄膜３中に存在する不純物７がポリシリコン薄膜６の表面層に集中する。このとき、ガラス基板１の温度を２００～４００℃とすると、凝固速度は室温の場合の６０～３０％に低減するので、結晶粒径の増大と共に不純物の表面層への一層の集中化を図ることができる。なお、波長３０８ｎｍのＸｅＣｌエキシマレーザのほかに、波長２４８ｎｍのＫｒＦ、波長１９３ｎｍのＡｒＦ、波長１７５ｎｍのＡｒＣｌ、波長３

５３ｎｍのＸｅＦ等のエキシマレーザを用いてもよいことはもちろんである。また、エキシマレーザ照射を複数回行えば、不純物の表面層への集中をより確実となすことができる。

【００１０】次に、ポリシリコン薄膜６の膜質を安定化するために、窒素雰囲気中において５００℃程度の温度で熱処理を行うと、図４（Ａ）に示すように、ポリシリコン薄膜６の表面に自然酸化膜８が形成される。次に、１％フッ酸に１分間程度浸し、エッチングを行う。すると、自然酸化膜８が数秒間程度で除去され、この後ポリシリコン薄膜６の表面層が１００Å程度除去される。この状態を図４（Ｂ）に示す。このように、ポリシリコン薄膜６の表面層を１００Å程度除去しているので、ポリシリコン薄膜６の表面層に集中して残留している不純物７も同時に除去されることになる。なお、ポリシリコン薄膜６の膜質を安定化するために、窒素雰囲気中ではなく、酸素雰囲気中において５００～６００℃程度の温度で熱処理を行ってもよい。この場合、窒素雰囲気中での熱処理の場合よりもエッチング時間を短縮することができるので、ガラス基板１に与えるダメージを少なくすることができる。また、エッチングはドライエッチングであってもよい。

【００１１】次に、図５に示すように、素子分離により、不要な部分のポリシリコン薄膜６を除去する。この状態では、ポリシリコン薄膜６の中央部はチャネル領域６ａとされ、その両側は活性化イオン注入領域からなるソース・ドレイン領域６ｂとされている。次に、図６に示すように、全表面に酸化シリコン膜と窒化シリコン膜とからなるゲート絶縁膜９を形成する。すなわち、まず全表面にスパッタにより酸化シリコン膜を堆積し、次いでこの酸化シリコン膜の表面にSiH_4とNH_3とN_2とからなる混合ガスを用いたプラズマＣＶＤにより窒化シリコン膜を堆積する。プラズマＣＶＤにより窒化シリコン膜を堆積する場合、ガラス基板１の温度を２５０℃程度とし、SiH_4を３０ＳＣＣＭ程度とし、NH_3を６０ＳＣＣＭ程度とし、N_2を３９０ＳＣＣＭ程度とし、出力６００Ｗ程度、圧力０．５Ｔｏｒｒ程度で行うと、同時にポリシリコン薄膜６が水素化されてそのダングリングボンドが減少する。このように、ポリシリコン薄膜６上にプラズマＣＶＤによりゲート絶縁膜９を堆積するのと同時にポリシリコン薄膜６を水素化してそのダングリングボンドを減らしているので、ゲート絶縁膜９の堆積とポリシリコン薄膜６の水素化を一度のプラズマＣＶＤで同時に行うことができ、したがって独自の水素化工程を省略することができ、ひいては製造工程数を少なくすることができる。次に、チャネル領域６ａに対応する部分のゲート絶縁膜９の上面にＣｒからなるゲート電極１０を形成する。

【００１２】次に、図７に示すように、全表面に窒化シリコン等からなる層間絶縁膜１１を形成する。次に、ソース・ドレイン領域６ｂに対応する部分の層間絶縁膜１１およびゲート絶縁膜９にコンタクトホール１２を形成する。次に、図７に示すように、コンタクトホール１２を介してソース・ドレイン領域６ｂと接続されるＡｌからなるソース・ドレイン電極１３を層間絶縁膜１１の上面にパターン形成する。かくして得られた電界効果型の薄膜トランジスタでは、オン電流、オフ電流、しきい値電圧等の電気的特性が向上し、移動度も８０ｃｍ²／Ｖ・ｓｅｃ以上であり、ポリシリコン薄膜６の膜質が極めて良好であることが確認された。

【００１３】なお、上記実施例では、プラズマＣＶＤにより水素化アモルファスシリコン薄膜２を堆積した後脱水素処理を行っているが、これに限定されるものではなく、例えばＬＰＣＶＤにより水素を含有しないアモルファスシリコン薄膜を堆積するようにしてもよい。この場合、ＬＰＣＶＤにより水素を含有しないアモルファスシリコン薄膜を堆積する際のガラス基板１の温度を５００～６００℃程度とし、ポリ化および活性化するためのエキシマレーザのエネルギ密度を４００ｍＪ／ｃｍ²程度とする。したがって、この場合には脱水素処理を行う必要はないが、ガラス基板１の温度を５００～６００℃程度と比較的高温とすることになるので、基板温度の昇温に時間が余計にかかることになる。また、ガラス基板１の温度を６００℃程度とした場合には、アモルファスシリコン薄膜ではなくポリシリコン薄膜が直接堆積されることになるが、その後のエキシマレーザ照射によりその結晶粒径が成長し、したがってポリシリコン薄膜の結晶構造を良くすることができる。

【００１４】また、上記実施例では、ポリ化と活性化を一度のエキシマレーザ照射で同時に行っているが、これは別々に行ってもよい。要は、ゲート絶縁膜９を形成する前に、レーザアニールによってポリシリコン薄膜の表面層に集中した不純物を除去することができればよい。このとき、ポリシリコン薄膜の膜質を安定化するための熱処理を行った場合には、ポリシリコン薄膜の表面に形成された自然酸化膜も除去される。

【００１５】また、上記実施例では、この発明を通常のＭＯＳ構造の薄膜トランジスタに適用した場合について説明したが、通常のＭＯＳ構造の薄膜トランジスタと比較して、耐圧の向上等を図って高信頼化したＬＤＤ構造の薄膜トランジスタにも適用することができる。例えば、図８と同一名称部分には同一の符号を付した図９に示すＬＤＤ構造の薄膜トランジスタでは、ポリシリコン薄膜６の中央部をチャネル領域６ａとされ、その両側をイオン濃度の低いソース・ドレイン領域６ｂとされ、さらにその両側をイオン濃度の高いソース・ドレイン領域６ｃとされた構造となっている。このＬＤＤ構造の薄膜トランジスタを製造する場合には、例えば図２に示すような状態において、イオン濃度の低いソース・ドレイン領域６ｂおよびイオン濃度の高いソース・ドレイン領域

６ｃを形成すべき部分に低濃度のイオンを注入し、次いでフォトレジスト膜４を除去し、次いでイオン濃度の高いソース・ドレイン領域６ｃを形成すべき部分以外の部分の上面に別のフォトレジスト膜を形成し、この別のフォトレジスト膜をマスクとしてイオン濃度の高いソース・ドレイン領域６ｃを形成すべき部分に高濃度のイオンを注入するようにすればよい。

【００１６】さらに、上記実施例では、この発明をトップゲート型のコプラナ構造の薄膜トランジスタに適用した場合について説明したが、スタガ構造やバックゲート型のコプラナまたはスタガ構造の薄膜トランジスタにも適用し得ることはもちろんである。バックゲート型の場合、ガラス基板の上面にゲート電極およびゲート絶縁膜を形成し、その上にアモルファスシリコン薄膜を堆積し、このアモルファスシリコン薄膜をポリ化してポリシリコン薄膜とする。また、ポリシリコン薄膜の水素化処理は、ポリシリコン薄膜上にパッシベーション膜（絶縁膜）をプラズマＣＶＤにより堆積する際に同時に行うことができる。

【００１７】

【発明の効果】以上説明したように、この発明によれば、半導体薄膜の表面層を該表面層に集中した不純物と共に除去しているので、半導体薄膜の膜質を良くすることができ、ひいてはオン電流、オフ電流、しきい値電圧等の電気的特性を向上することができる。

【図面の簡単な説明】

【図１】この発明の一実施例における薄膜トランジスタの製造に際し、ガラス基板の上面に水素化アモルファスシリコン薄膜を堆積した状態の断面図。

【図２】同薄膜トランジスタの製造に際し、脱水素処理後のアモルファスシリコン薄膜のソース・ドレイン形成領域にイオンを注入した状態の断面図。

【図３】同薄膜トランジスタの製造に際し、エキシマレーザを照射することにより、アモルファスシリコン薄膜をポリ化すると同時にイオン注入領域を活性化した状態の断面図。

【図４】（Ａ）は同薄膜トランジスタの製造に際し、熱処理により、ポリシリコン薄膜の表面に自然酸化膜を形成した状態の断面図、（Ｂ）は同薄膜トランジスタの製造に際し、エッチングにより、ポリシリコン薄膜の表面層を除去した状態の断面図。

【図５】同薄膜トランジスタの製造に際し、素子分離により、不要な部分のポリシリコン薄膜を除去した状態の断面図。

【図６】同薄膜トランジスタの製造に際し、ゲート絶縁膜およびゲート電極を形成した状態の断面図。

【図７】同薄膜トランジスタの製造に際し、層間絶縁膜をおよびコンタクトホールを形成した状態の断面図。

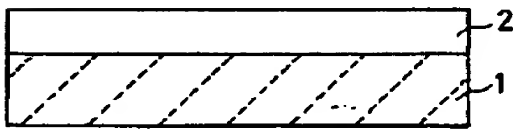
【図８】同薄膜トランジスタの製造に際し、ソース・ドレイン電極を形成した状態の断面図。

【図９】この発明をＬＤＤ構造の薄膜トランジスタに適用した場合の図８同様の断面図。

【符号の説明】

1　ガラス基板
3　アモルファスシリコン薄膜
6　ポリシリコン薄膜
7　不純物
8　自然酸化膜

【図１】



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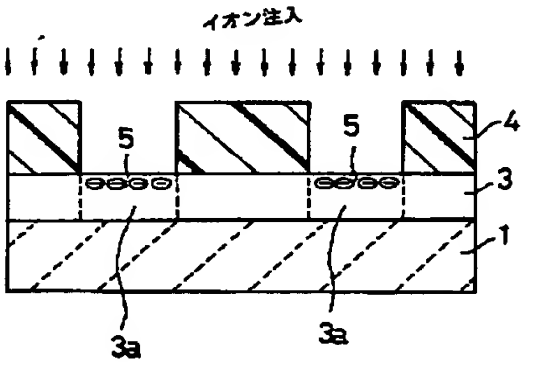

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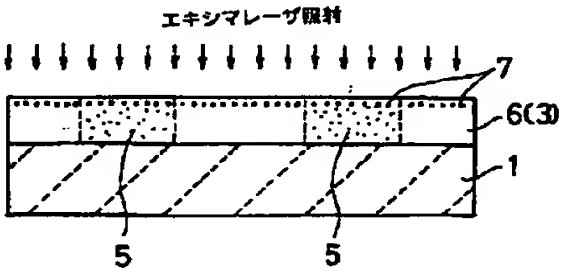

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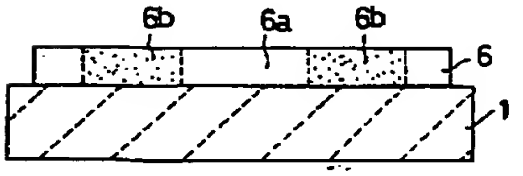

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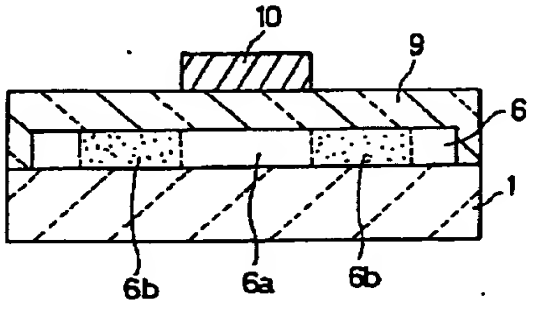

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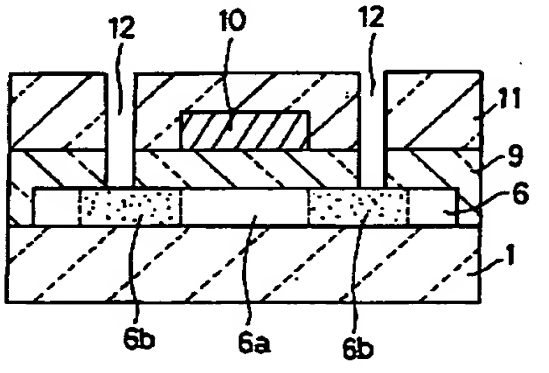

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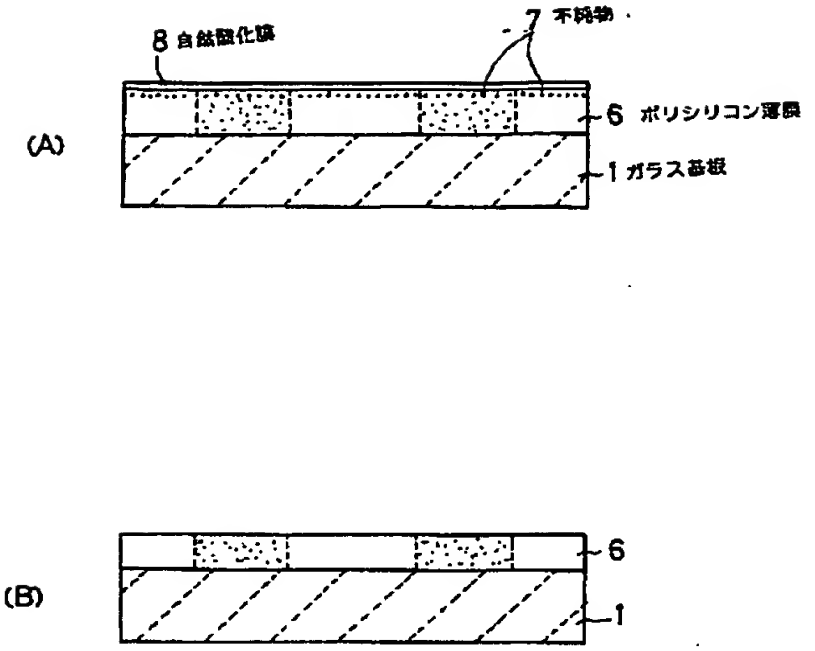

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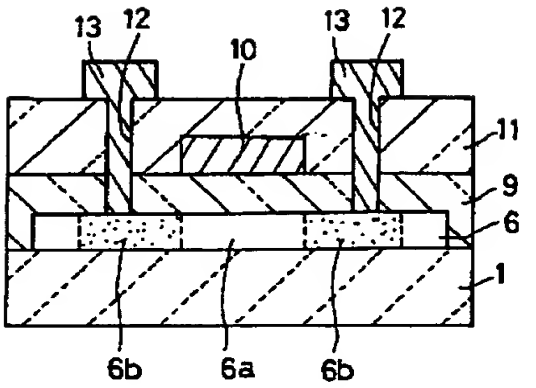

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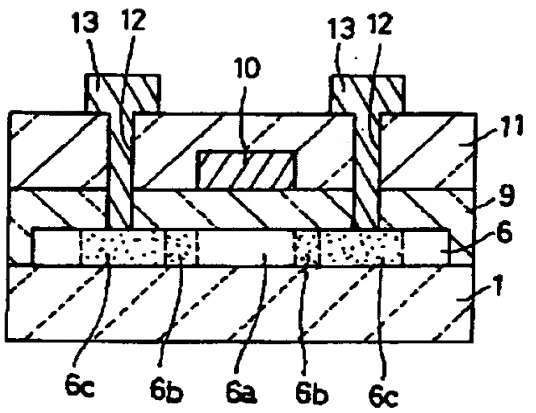

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(71)Applicant : CASIO COMPUT CO LTD

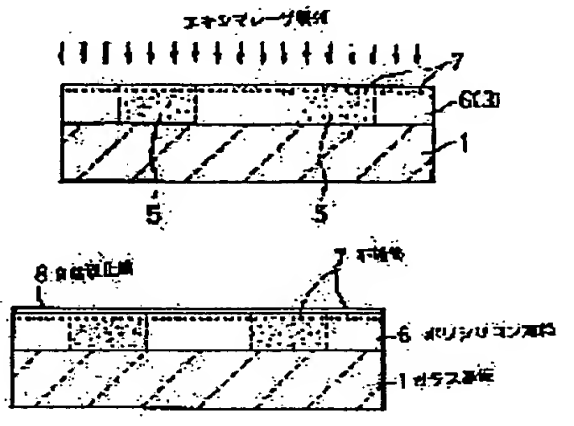
(72)Inventor : MOROSAWA KATSUHIKO

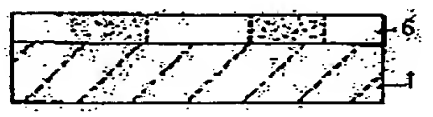
(54) MANUFACTURE OF THIN FILM TRANSISTOR

(57)Abstract:

PURPOSE: To improve the film quality of a semiconductor film by removing the impurities collected on the surface layer together with the surface layer of the semiconductor film after the semiconductor film formed on a substrate has been laser-annealed.

CONSTITUTION: The impurities 7 present in an amorphous silicon thin film 3 are concentrated on the surface of a polysilicon thin film 6 by solidifying from the side of a substrate 1, the amorphous silicon thin film 3 which is fused by laser annealing. A natural oxide film 8 is formed on the surface of the polysilicon thin film 6 when heat treatment is conducted in a nitrogen atmosphere. Then, the above-mentioned material is dipped into 1% fluoric acid for one minute, and etching treatment is conducted. As a result, the natural oxide film 8 is removed in about several seconds, and 100Å or thereabout of the surface of the polysilicon thin film 6 is removed. Consequently, the impurities 7 which are concentrated on the surface layer of the polysilicon thin film 6 are removed simultaneously. Accordingly, the film quality of the polysilicon thin film 6 can be stabilized.





LEGAL STATUS

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[Date of final disposal for application]

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[Date of registration]	29.11.2002
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[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the thin film transistor characterized by removing with the impurity which concentrated the surface layer of said semi-conductor thin film on this surface layer after carrying out laser annealing of the semi-conductor thin film formed on the substrate.
[Claim 2] Said semi-conductor thin film is the manufacture approach of the thin film transistor according to claim 1 which is said before [laser annealing] amorphous silicon thin film, and is characterized by Pori-izing this amorphous silicon thin film by said laser annealing.
[Claim 3] The manufacture approach of the thin film transistor according to claim 1 characterized by heat-treating after said laser annealing and removing the surface layer of said semi-conductor thin film after this.
[Claim 4] It is the manufacture approach of the thin film transistor according to claim 3 characterized by performing said heat treatment in nitrogen-gas-atmosphere mind.
[Claim 5] It is the manufacture approach of the thin film transistor according to claim 3 characterized by performing said heat treatment in an oxygen ambient atmosphere.

[Translation done.]

NOTICES *

DETAILED DESCRIPTION

Detailed Description of the Invention]
0001]
Industrial Application] This invention relates to the manufacture approach of a thin film transistor.
0002]
Description of the Prior Art] In the manufacture field of a thin film transistor, by carrying out laser annealing, the amorphous silicon thin film formed on the glass substrate may be Pori-ized, and may be used as a polish recon thin film. In this case, the amorphous silicon thin film fused by laser annealing solidifies and Pori-izes from a glass substrate side. Moreover, although laser annealing of the polish recon thin film after an ion implantation may be carried out and it may be activated, the polish recon thin film fused by laser annealing also in this case solidifies from a glass substrate side.
[0003]
[Problem(s) to be Solved by the Invention] Thus, since the semi-conductor thin film which consists of an amorphous silicon thin film fused by laser annealing solidifies from a glass substrate side, the impurity which exists in a semi-conductor thin film will focus on the surface layer, and will remain. Consequently, in the thin film transistor equipped with the semi-conductor thin film of such structure, there was a problem that electrical characteristics, such as the ON state current, the OFF state current, and a threshold electrical potential difference, deteriorated with the not sufficient membraneous quality of a semi-conductor thin film. The purpose of this invention is to offer the manufacture approach of the thin film transistor which can improve membraneous quality of a semi-conductor thin film.
[0004]
[Means for Solving the Problem] This invention is removed with the impurity which concentrated the surface layer of said semi-conductor thin film on this surface layer, after carrying out laser annealing of the semi-conductor thin film formed on the substrate.
[0005]
[Function] Since it will remove with the impurity which concentrated the surface layer of a semi-conductor thin film on this surface layer according to this invention, membraneous quality of a semi-conductor thin film can be improved.
[0006]
[Example] Drawing 1 - drawing 8 show each production process of the thin film transistor in one example of this invention, respectively. Then, the manufacture approach of a thin film transistor is explained, referring to these drawings in order.
[0007] First, as shown in drawing 1 , the hydrogenation amorphous silicon thin film 2 is deposited on the top face of a glass substrate 1 by the plasma CVD which used the mixed gas of SiH4 and H2. In this case, it is made for the thickness of the hydrogenation amorphous silicon thin film 2 to become to some extent thicker than the thickness made into the purpose. For example, if the target thickness is about 500A, it may be plus 100A about 600A. Moreover, as deposition conditions, about 200-350 degrees C of temperature of a glass substrate 1 are desirably made into about 250 degrees C, and the mixed gas of SiH4 of 10 - 20SCCM extent and Hthe about 10 times 2 is used. Then, the hydrogen content of the hydrogenation amorphous silicon thin film 2 becomes about 10-20atomic%. Next, dehydrogenation treatment is performed in order to avoid that hydrogen bumps and a defect arises, when high energy is given by excimer laser exposure at a next process. in this case, the inside of nitrogen-gas-atmosphere mind -- setting -- the temperature of about 450 degrees C -- heat treatment of about 1 hour -- carrying out -- a hydrogen content -- less than [3atomic%] -- it is made to become less than [1atomic%] desirably
[0008] Next, as shown in drawing 2 , the photoresist film 4 is formed in the top face of the part corresponding to fields other than source drain formation field 3a of the amorphous silicon thin film 3 after dehydrogenation treatment. Next, ion, such as phosphorus ion and boron ion, is poured into source drain formation field 3a of the amorphous silicon thin film 3 by using this photoresist film 4 as a mask, and the ion-implantation field 5 is formed. Then, the photoresist film 4 is removed.
[0009] Next, while the amorphous silicon thin film 3 will Pori-ize and will turn into the polish recon thin film 6 if XeCl

excimer laser with a wavelength of 308 is irradiated at the substrate temperature of 200-400 degrees C into a vacuum by the energy density 250 - about two 350 mJ/cm, and about 50ns of pulse width as shown in drawing 3 , the ion-implantation field 5 is activated. In this case, when the amorphous silicon thin film 3 fused by laser annealing solidifies from a glass substrate 1 side, the impurity 7 which exists in the amorphous silicon thin film 3 focuses on the surface layer of the polish recon thin film 6. If temperature of a glass substrate 1 is made into 200-400 degrees C at this time, since a coagulation rate will be reduced to 60 - 30% in the case of a room temperature, much more centralization to the surface layer of an impurity can be attained with increase of the diameter of crystal grain. In addition, of course, excimer laser other than XeCl excimer laser with a wavelength of 308nm, such as KrF with a wavelength of 248nm, ArF with a wavelength of 193nm, ArCl with a wavelength of 175nm, and XeF with a wavelength of 353nm, may be used. Moreover, if a excimer laser exposure is performed two or more times, the surface layer of an impurity can be concentrated as it is more certain.

[0010] Next, if it heat-treats at the temperature of about 500 degrees C in nitrogen-gas-atmosphere mind in order to stabilize the membraneous quality of the polish recon thin film 6, as shown in drawing 4 (A), the natural oxidation film 8 will be formed in the front face of the polish recon thin film 6. Next, it etches by dipping in fluoric acid a grade for 1 minute 1%. Then, the natural oxidation film 8 is removed by several second about room, and about 100A of surface layers of the polish recon thin film 6 is removed after this. This condition is shown in drawing 4 (B). Thus, since about 100A of surface layers of the polish recon thin film 6 is removed, the impurity 7 which focused on the surface layer of the polish recon thin film 6, and remains will also be removed by coincidence. In addition, in order to stabilize the membraneous quality of the polish recon thin film 6, you may heat-treat at the temperature of about 500-600 degrees C not in nitrogen-gas-atmosphere mind but in an oxygen ambient atmosphere. In this case, since etching time can be shortened rather than the case of heat treatment in nitrogen-gas-atmosphere mind, the damage given to a glass substrate can be lessened. Moreover, etching may be dry etching.

[0011] Next, as shown in drawing 5 , isolation removes the polish recon thin film 6 of an unnecessary part. In this condition, the center section of the polish recon thin film 6 is set to channel field 6a, and those both sides are set to source drain field 6b which consists of an activation ion-implantation field. Next, as shown in drawing 6 , the gate dielectric film 9 which consists of silicon oxide film and a silicon nitride film is formed in all front faces.

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention relates to the manufacture approach of a thin film transistor.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] In the manufacture field of a thin film transistor, by carrying out laser annealing, the amorphous silicon thin film formed on the glass substrate may be Pori-ized, and may be used as a polish recon thin film. In this case, the amorphous silicon thin film fused by laser annealing solidifies and Pori-izes from a glass substrate side. Moreover, although laser annealing of the polish recon thin film after an ion implantation may be carried out and it may be activated, the polish recon thin film fused by laser annealing also in this case solidifies from a glass substrate side.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] Since it has removed with the impurity which concentrated the surface layer of a semiconductor thin film on this surface layer according to this invention as explained above, membraneous quality of a semiconductor thin film can be improved, as a result electrical characteristics, such as the ON state current, the OFF state current, and a threshold electrical potential difference, can be improved.

[Translation done.]

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Thus, since the semi-conductor thin film which consists of an amorphous silicon thin film fused by laser annealing solidifies from a glass substrate side, the impurity which exists in a semi-conductor thin film will focus on the surface layer, and will remain. Consequently, in the thin film transistor equipped with the semi-conductor thin film of such structure, there was a problem that electrical characteristics, such as the ON state current, the OFF state current, and a threshold electrical potential difference, deteriorated with the not sufficient membraneous quality of a semi-conductor thin film. The purpose of this invention is to offer the manufacture approach of the thin film transistor which can improve membraneous quality of a semi-conductor thin film.

[Translation done.]

MEANS

[Means for Solving the Problem] This invention is removed with the impurity which concentrated the surface layer of said semi-conductor thin film on this surface layer, after carrying out laser annealing of the semi-conductor thin film formed on the substrate.
[0005]

[Translation done.]

OPERATION

[Function] Since it will remove with the impurity which concentrated the surface layer of a semi-conductor thin film on this surface layer according to this invention, membraneous quality of a semi-conductor thin film can be improved.

[Translation done.]

EXAMPLE

[Example] Drawing 1 - drawing 8 show each production process of the thin film transistor in one example of this invention, respectively. Then, the manufacture approach of a thin film transistor is explained, referring to these drawings in order.

[0007] First, as shown in drawing 1 , the hydrogenation amorphous silicon thin film 2 is deposited on the top face of a glass substrate 1 by the plasma CVD which used the mixed gas of SiH4 and H2. In this case, it is made for the thickness of the hydrogenation amorphous silicon thin film 2 to become to some extent thicker than the thickness made into the purpose. For example, if the target thickness is about 500A, it may be plus 100A about 600A. Moreover, as deposition conditions, about 200-350 degrees C of temperature of a glass substrate 1 are desirably made into about 250 degrees C, and the mixed gas of SiH4 of 10 - 20SCCM extent and Hthe about 10 times 2 is used. Then, the hydrogen content of the hydrogenation amorphous silicon thin film 2 becomes about 10-20atomic%. Next, dehydrogenation treatment is performed in order to avoid that hydrogen bumps and a defect arises, when high energy is given by excimer laser exposure at a next process. in this case, the inside of nitrogen-gas-atmosphere mind -- setting -- the temperature of about 450 degrees C -- heat treatment of about 1 hour -- carrying out -- a hydrogen content -- less than [3atomic%] -- it is made to become less than [1atomic%] desirably

[0008] Next, as shown in drawing 2 , the photoresist film 4 is formed in the top face of the part corresponding to fields other than source drain formation field 3a of the amorphous silicon thin film 3 after dehydrogenation treatment. Next, ion, such as phosphorus ion and boron ion, is poured into source drain formation field 3a of the amorphous silicon thin film 3 by using this photoresist film 4 as a mask, and the ion-implantation field 5 is formed. Then, the photoresist film 4 is removed.

[0009] Next, while the amorphous silicon thin film 3 will Pori-ize and will turn into the polish recon thin film 6 if XeCl excimer laser with a wavelength of 308nm is irradiated at the substrate temperature of 200-400 degrees C into a vacuum by the energy density 250 - about two 350 mJ/cm, and about 50ns of pulse width as shown in drawing 3 , the ion-implantation field 5 is activated. In this case, when the amorphous silicon thin film 3 fused by laser annealing solidifies from a glass substrate 1 side, the impurity 7 which exists in the amorphous silicon thin film 3 focuses on the surface layer of the polish recon thin film 6. If temperature of a glass substrate 1 is made into 200-400 degrees C at this time, since a coagulation rate will be reduced to 60 - 30% in the case of a room temperature, much more centralization to the surface layer of an impurity can be attained with increase of the diameter of crystal grain. In addition, of course, excimer laser other than XeCl excimer laser with a wavelength of 308nm, such as KrF with a wavelength of 248nm, ArF with a wavelength of 193nm, ArCl with a wavelength of 175nm, and XeF with a wavelength of 353nm, may be used. Moreover, if a excimer laser exposure is performed two or more times, the surface layer of an impurity can be concentrated as it is more certain.

[0010] Next, if it heat-treats at the temperature of about 500 degrees C in nitrogen-gas-atmosphere mind in order to stabilize the membraneous quality of the polish recon thin film 6, as shown in drawing 4 (A), the natural oxidation film 8 will be formed in the front face of the polish recon thin film 6. Next, it etches by dipping in fluoric acid a grade for 1 minute 1%. Then, the natural oxidation film 8 is removed by several second about room, and about 100A of surface layers of the polish recon thin film 6 is removed after this. This condition is shown in drawing 4 (B). Thus, since about 100A of surface layers of the polish recon thin film 6 is removed, the impurity 7 which focused on the surface layer of the polish recon thin film 6, and remains will also be removed by coincidence. In addition, in order to stabilize the membraneous quality of the polish recon thin film 6, you may heat-treat at the temperature of about 500-600 degrees C not in nitrogen-gas-atmosphere mind but in an oxygen ambient atmosphere. In this case, since etching time can be shortened rather than the case of heat treatment in nitrogen-gas-atmosphere mind, the damage given to a glass substrate 1 can be lessened. Moreover, etching may be dry etching.

[0011] Next, as shown in drawing 5 , isolation removes the polish recon thin film 6 of an unnecessary part. In this condition, the center section of the polish recon thin film 6 is set to channel field 6a, and those both sides are set to source drain field 6b which consists of an activation ion-implantation field. Next, as shown in drawing 6 , the gate

dielectric film 9 which consists of silicon oxide film and a silicon nitride film is formed in all front faces. That is, the silicon oxide film is first deposited on all front faces by the spatter, and a silicon nitride film is deposited by the plasma CVD using the mixed gas which consists of SiH4, and NH3 and N2 subsequently to the front face of this silicon oxide film. If make temperature of a glass substrate 1 into about 250 degrees C, make SiH4 into 30SCCM extent, NH3 is made into 60SCCM extent, N2 is made into 390SCCM extent and it carries out about output 600W and with pressure 0.5Torr extent when depositing a silicon nitride film by plasma CVD, the polish recon thin film 6 will be hydrogenated by coincidence, and the dangling bond will decrease in number. Thus, since the polish recon thin film 6 is hydrogenated to depositing gate dielectric film 9 by plasma CVD on the polish recon thin film 6, and coincidence and the dangling bond is reduced, deposition of gate dielectric film 9 and hydrogenation of the polish recon thin film 6 can be once performed to coincidence by plasma CVD, an original hydrogenation process can be skipped, as a result the number of production processes can be lessened. Next, the gate electrode 10 which consists of Cr is formed in the top face of the gate dielectric film 9 of the part corresponding to channel field 6a.

[0012] Next, as shown in drawing 7 , the interlayer insulation film 11 which consists of silicon nitride etc. is formed in all front faces. Next, a contact hole 12 is formed in the interlayer insulation film 11 and gate dielectric film 9 of a part corresponding to source drain field 6b. Next, as shown in drawing 7 , pattern formation of the source drain electrode 13 which consists of aluminum connected with source drain field 6b through a contact hole 12 is carried out to the top face of an interlayer insulation film 11. In the thin film transistor of the electric field effect mold obtained in this way, electrical characteristics, such as the ON state current, the OFF state current, and a threshold electrical potential difference, improved, mobility is also more than 80cm2/V-sec, and it was checked that the membraneous quality of the polish recon thin film 6 is very good.

[0013] In addition, although dehydrogenation treatment is performed in the above-mentioned example after depositing the hydrogenation amorphous silicon thin film 2 by plasma CVD, it is not limited to this and you may make it deposit the amorphous silicon thin film which does not contain hydrogen by LPCVD. In this case, temperature of the glass substrate 1 at the time of depositing the amorphous silicon thin film which does not contain hydrogen by LPCVD is made into about 500-600 degrees C, and the energy density of Pori-izing and the excimer laser for being activated is made into about two 400 mJ/cm. Therefore, although it is not necessary to perform dehydrogenation treatment in this case, since temperature of a glass substrate 1 will be comparatively made into an elevated temperature with about 500-600 degrees C, time amount becomes this thing to the temperature up of substrate temperature too many. Moreover, although not an amorphous silicon thin film but a polish recon thin film will accumulate directly when temperature of a glass substrate 1 is made into about 600 degrees C, the diameter of crystal grain can grow by subsequent excimer laser exposure, therefore the crystal structure of a polish recon thin film can be improved.

[0014] Moreover, although the above-mentioned example is performing Pori-izing and activation to coincidence by the excimer laser exposure once, this is separately good in a line. What is necessary is in short, just to be able to remove the impurity concentrated on the surface layer of a polish recon thin film by laser annealing, before forming gate dielectric film 9. When heat treatment for stabilizing the membraneous quality of a polish recon thin film is performed at this time, the natural oxidation film formed in the front face of a polish recon thin film is also removed.

[0015] Moreover, although the above-mentioned example explained the case where this invention was applied to the thin film transistor of the usual metal-oxide-semiconductor structure, as compared with the thin film transistor of the usual metal-oxide-semiconductor structure, it is applicable also to the thin film transistor of the LDD structure which aimed at and formed improvement in pressure-proofing etc. into high reliance. For example, in the thin film transistor of the LDD structure shown in drawing 9 which gave the same sign to the same name part as drawing 8 , it has structure which was set to channel field 6a in the center section of the polish recon thin film 6, was set to source drain field 6b with low ion concentration in the both sides, and was further set to source drain field 6c with high ion concentration in the both sides. In manufacturing the thin film transistor of this LDD structure For example, low-concentration ion is injected into the part which should form source drain field 6b with low ion concentration, and source drain field 6c with high ion concentration in the condition that it is shown in drawing 2 . Subsequently, remove the photoresist film 4 and another photoresist film is formed in the top face of parts other than the part which should form source drain field 6c with ion concentration high subsequently. What is necessary is just to make it inject high-concentration ion into the part which should form source drain field 6c with high ion concentration by using this another photoresist film as a mask.

[0016] Furthermore, although the above-mentioned example explained the case where this invention was applied to the thin film transistor of the coplanar structure of a top gate mold, as for coplanar **** of stagger structure or a backgate mold, it is needless to say that it can apply also to the thin film transistor of stagger structure. In the case of a backgate mold, a gate electrode and gate dielectric film are formed in the top face of a glass substrate, an amorphous silicon thin film is deposited on it, this amorphous silicon thin film is Pori-ized, and it considers as a polish recon thin film. Moreover, in case the hydrogen treating of a polish recon thin film deposits the passivation film (insulator layer) by plasma CVD on a polish recon thin film, it can be performed to coincidence.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view in the condition of having deposited the hydrogenation amorphous silicon thin film on the top face of a glass substrate on the occasion of manufacture of the thin film transistor in one example of this invention.
[Drawing 2] The sectional view in the condition of having poured ion into the source drain formation field of the amorphous silicon thin film after dehydrogenation treatment on the occasion of manufacture of this thin film transistor.
[Drawing 3] The sectional view in the condition of having activated the ion-implantation field while Pori-izing the amorphous silicon thin film by irradiating excimer laser on the occasion of manufacture of this thin film transistor.
[Drawing 4] For (A), on the occasion of manufacture of this thin film transistor, (B) is a sectional view in the condition of having formed the natural oxidation film in the front face of a polish recon thin film by heat treatment, and a sectional view in the condition that etching removed the surface layer of a polish recon thin film, on the occasion of manufacture of this thin film transistor.
[Drawing 5] The sectional view in the condition that isolation removed the polish recon thin film of an unnecessary part on the occasion of manufacture of this thin film transistor.
[Drawing 6] The sectional view in the condition of having formed gate dielectric film and a gate electrode on the occasion of manufacture of this thin film transistor.
[Drawing 7] The sectional view in the condition of having reached the interlayer insulation film and having formed the contact hole on the occasion of manufacture of this thin film transistor.
[Drawing 8] The sectional view in the condition of having formed the source drain electrode on the occasion of manufacture of this thin film transistor.
[Drawing 9] The same sectional view as drawing 8 at the time of applying this invention to the thin film transistor of LDD structure.
[Description of Notations]
1 Glass Substrate
3 Amorphous Silicon Thin Film
6 Polish Recon Thin Film
7 Impurity
8 Natural Oxidation Film

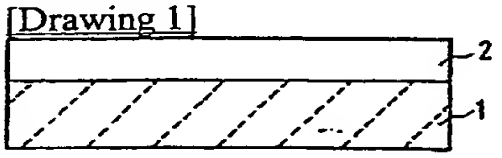
[Translation done.]

* NOTICES *

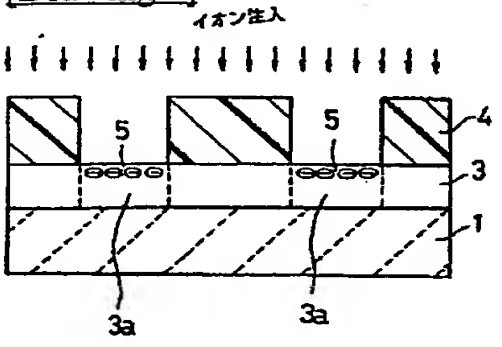
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

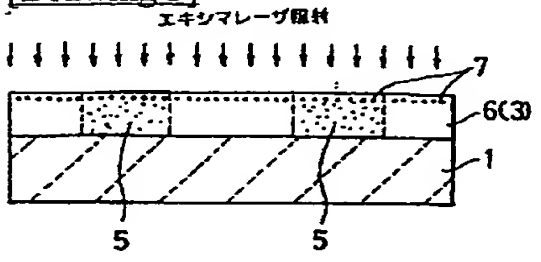
[Drawing 1]



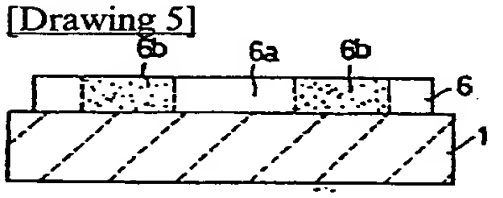
[Drawing 2]



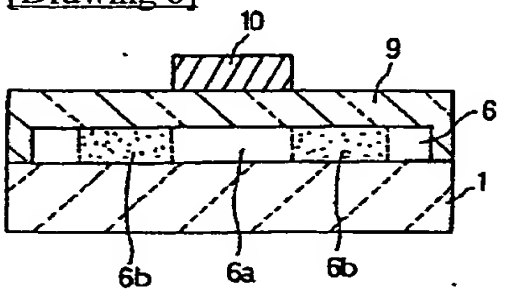
[Drawing 3]



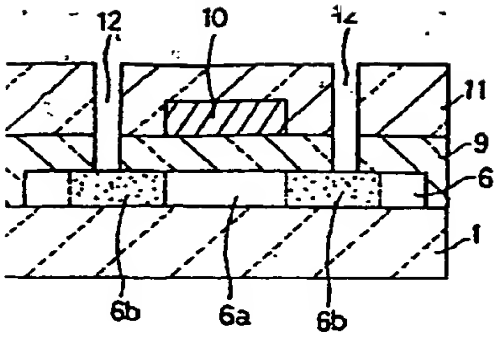
[Drawing 5]



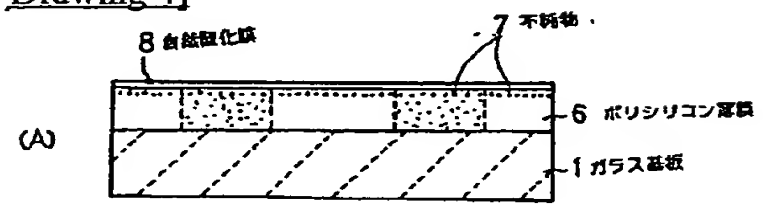
[Drawing 6]

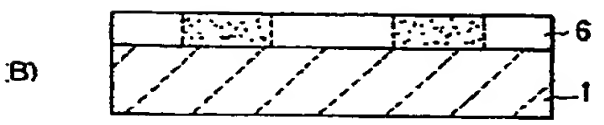


[Drawing 7]

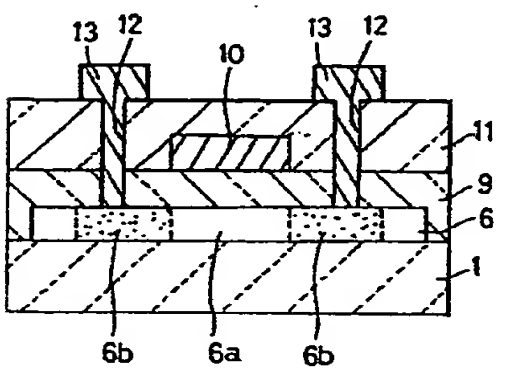


[Drawing 4]

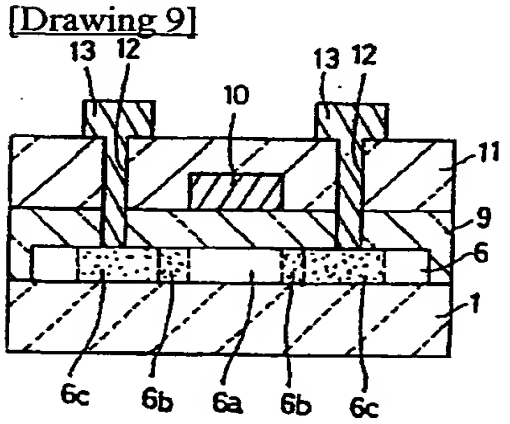




[Drawing 8]



[Drawing 9]



[Translation done.]